REMARKS

Currently, Claims 15-34 are pending in the above application and stand rejected under the Office Action mailed September 13, 2001. This Office Action is the first action in a continued prosecution application, but is a final Office Action. The Examiner's consideration of the enclosed amendment is respectfully requested.

Supplemental Information Disclosure Statements:

The Examiner is requested to acknowledge receipt and consideration of supplemental Information Disclosure Statements submitted in this application on May 30, 2001, and June 1, 2001.

Introduction to Disclosed Embodiments of the Present Invention:

The present invention provides methods for depositing noble metals onto surfaces of microelectronic workpieces. The method is carried out in preferred embodiments using apparatus that have conventionally been used for depositing copper, but have not heretofore been successfully used for deposition of noble metals. In accordance with aspects of the disclosed invention, electroplating power is applied to a workpiece in this apparatus for a first time period at a first low current followed by additional deposition for a second time period at a second low current. This sequence has been found to result in deposition of noble metal films, such as platinum films, that avoid the overstress and other problems associated with conventional platinum plating.

Amendment to the Claims:

Claim 15 has been amended above to clarify certain aspects of the present invention. First, it is noted that the claimed method is a method for electroplating a noble metal into submicron features, the noble metal being deposited into the submicron features during the first

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and second time periods of current application. Support for deposition of platinum into submicron features is found at page 22, line 10.

Claim 15 has also been amended to reflect that this noble metal is deposited onto a surface as prepared with a metal seed layer of no more than 1000 angstroms thick. Support for this recitation is found at page 2, lines 14-15.

Rejection Under 35 U.S.C. § 103:

Claim 15 stands rejected based on a hypothetical combination of three references. The primary reference is U.S. Patent No. 6,132,587 to Jorne et al., which is cited for disclosing the overall concept of positioning a wafer face down opposite an anode and contacting the surface with an electroplating solution. As noted by the Examiner, Jorne et al. discloses the deposition of copper in this manner. However it is respectfully noted that Jorne et al. does not disclose or suggest in any way that this technique may be utilized for noble metal deposition. Nor does Jorne et al. disclose or suggest in any way the deposition of any metal using a low current density for a first period of time and a higher current density for a second period of time. These distinctions are noted by the Examiner.

For the deposition of noble metals, the Examiner looks to either U.S. Patent No. 5,556,814 to Inoue et al. or U.S. Patent No. 5,549,808 to Farooq et al. Inoue et al. and Farooq et al. do both disclose electrochemical deposition of noble metals. However, it is not electrochemical deposition in the manner claimed. Inoue et al., for instance, discloses the formation of wiring using deposition of a lower wiring 3 (Figure 6), followed by deposition of a second wiring 25 (Figure 7), which may include a noble metal, and which has a thickness of 5 to 100 nm thick (column 4, lines 37-38), followed by deposition of an undermetal layer 26 (FIGURE 8) which has a thickness ranging from 30 nm to 300 nm (column 4, lines 55-56), followed by a noble metal top layer plated wiring 28 having a thickness of 1 micron to 2 microns

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(column 5, lines 10-16), which may be a noble metal. Inoue et al. is directed to formation of wiring having a line width of approximately 10 microns (column 4, lines 38-41), rather than to deposition of noble metals into submicron features. Further, Inoue et al. does not disclose the deposition of noble metals onto a seed layer of less than 1000 angstroms. Further, there is no suggestion or disclosure in Inoue et al. to adapt any methods disclosed therein for use in an apparatus such as disclosed in Jorne et al.

The alternate secondary reference relied upon for disclosure of noble metal plating is Farooq et al. Farooq et al. is also directed to a process different than disclosed. Specifically, Farooq is directed to methods of capping copper electrical interconnects. It is the capping layer 23 that may be formed from noble metals (column 4, lines 53-57). The copper interconnect onto which the noble metal capping layer is deposited has a thickness of between 0.5 micron and 1000 microns (preferably between 2 microns and 25 microns). (Column 4, lines 23-26.) Thus Farooq et al. fails to disclose deposition of a noble metal onto a seed layer of no more than 1000 angstroms. Further, Farooq et al. is not directed to deposition of noble metals into submicron features. Further, again, there is no disclosure or suggestion in Farooq et al. to deposit noble metals using the techniques and apparatus disclosed in Jorne et al.

In summary, applicants respectfully note that there is no suggestion in the art to combine either Farooq et al. or Inoue et al. with Jorne et al. in the manner set forth in the Office Action. Without such a teaching or suggestion in the art, such combination is improper. However, even if, *arguendo*, such a teaching or suggestion is assumed, these combinations would not result in the methods of depositing noble metals that are claimed, as noted above.

The additional aspect of the present invention, also recognized by the Examiner as not being disclosed by Jorne et al., is carrying out plating at a first low current density followed by a second current density. For this, the Examiner relies on U.S. Patent No. 6,074,544 to Reid et al.,

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or U.S. Patent No. 6,140,241 to Shue et al., or the Lowenheim text. Applicants respectfully submit that Reid et al. is directed to deposition of copper, rather than noble metals (see column 3, lines 43-57). Shue et al. likewise is directed to deposition of copper (see abstract). The Lowenheim text is directed to general electroplating techniques, rather than semiconductor techniques specifically, and seems to be bent towards deposition of conductive metal coatings on plastics (page 17), which after deposition of these metalizing coatings on a nonconductive substrate, they are polished or buffed (page 418).

None of these references are directed to noble metal deposition, and none of them teach or suggest carrying out noble metal deposition as recited in the methods claimed, or combining their teachings with the teachings of Jorne et al. Thus addition of these references also fails to result in the claimed invention.

Applicants therefore respectfully request that the Examiner withdraw the rejection of Claim 15, which is submitted to be patentable over any hypothetical combination of the references set forth in the Office Action. Likewise, all claims dependent from Claim 15 are also submitted to be patentable over these references, and thus the additional rejections of dependent claims are not further addressed.

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CONCLUSION

In view of the above amendment and remarks, reconsideration and passage of the application inclusive of Claims 15-34 is respectfully requested.

Respectfully submitted,

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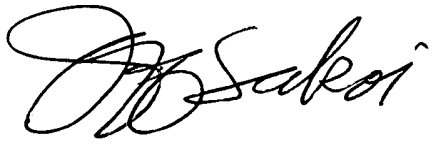

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I hereby certify that this correspondence is being deposited with the U.S. Postal Service in a sealed envelope as first class mail with postage thereon fully prepaid and addressed to the Commissioner for Patents, Washington, D.C. 20231, on the below date.

Date: October 11, 2001

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VERSION WITH MARKINGS TO SHOW CHANGES MADE OCTOBER 11, 2001

In the Specification:

The paragraph beginning on page 14, line 10, has been amended as follows:

FIGURES [11]11A, 11B and 12 illustrate two different embodiments of a "Belleville ring" contact structure.

The paragraph beginning on page 14, line 17, has been amended as follows:

FIGURES [16B - 20]16B, 17, 18A, 19A-19C and 20A-20D illustrate various aspects of one embodiment of a quick-attach mechanism.

The paragraph beginning on page 18, line 11, has been amended as follows:

It will be recognized that other reactor assembly configurations may be used with the inventive aspects of the disclosed reactor head, the foregoing being merely illustrative. Another reactor assembly suitable for use in the foregoing configuration is illustrated in U.S.S.N.[_____] 60/143,769, entitled "Workpiece Processor Having Improved Processing Chamber", filed July 12, 1999[(Attorney Docket No. SEM4492P0831US)], and a further reactor assembly is illustrated in U.S.S.N. 60/120,955, filed April 13, 1999, both of which are incorporated herein by reference.

The paragraph beginning on page 53, line 2, has been amended as follows:

FIGURES 26 through 28 are top plan views of integrated processing tools, shown generally at 1450, 1455, and 1500 that may be used to deposit a noble metal on the surface of a microelectronic workpiece, such as a semiconductor wafer. Processing tools 1450 and 1455 are each based on tool platforms developed by Semitool, Inc., of Kalispell, Montana. The processing tool platform of the tool 1450 is sold under the trademark

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LT-210™, the processing tool platform of the tool 1455 is sold under the trademark LT-210C™, and the processing tool 1500 is sold under the trademark EQUINOX™. The principal difference between the tools 1450, 1455 is in the footprints required for each. The platform on which tool 1455 is based has a smaller footprint than the platform on which tool [1455]1450 is based. Additionally, the platform on which tool 1450 is based is modularized and may be readily expanded. Each of the processing tools 1450, 1455, and 1500 are computer programmable to implement user entered processing recipes.

In the Claims:

15. (Amended) A method for electroplating a noble metal into submicron features on a surface of a microelectronic workpiece, the method comprising the steps of:

bringing the surface of the workpiece that is to be plated into contact with an electroplating solution including ions and/or complexes of a noble metal that is to be plated on the surface of the workpiece, the surface being prepared with a metal seed layer of no more than 1000 Angstroms thick;

providing an anode spaced from the surface of the workpiece [support]and contacting the electroplating solution[.];

applying electroplating power between the surface of the workpiece and the anode using a low current for a first predetermined period of time;

applying higher current electroplating power between the surface of the workpiece and the anode for a second predetermined period of time, the noble metal being deposited into the submicron features during the first and second time periods;

halting application of electroplating power; and

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disengaging the surface of the workpiece from the electroplating solution.

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